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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/779,683 | 02/18/2004 | Masahiro Kanai | 118739 | 8559 |

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| EXAMINER | |
|---|---|
| SOFOCLEOUS, ALEXANDER | |
| **ART UNIT** | **PAPER NUMBER** |
| 2824 | |

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/779,683 | KANAI, MASAHIRO | |
| | Examiner | Art Unit | |
| | Alexander Sofocleous | 2824 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date */3) 2/18,8/11/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

## DETAILED ACTION

1. This action is responsive to the following communications: the Application filed on February 18, 2004, the Information Disclosure Statement filed on February 18, 2004, the Information Disclosure Statement filed on August 11, 2004, and Foreign Priority filed on February 18, 2004.

2. Claims 1-13 are pending in the case. Claim 1 is an independent claim.

### *Priority*

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been received in Application.

### *Information Disclosure Statement*

4. The document number for 28 has been crossed-through on Applicant's IDS submitted 8/11/2004 because the mailroom stamp covers portions of the document number. Examiner assumes that applicant intended for 28 to be U.S. Application Publication 2003/0198102A1 and has considered and added to Form 892.

5. The following document numbers have been crossed-through on Applicant's IDS submitted 8/11/2004 and have been considered and added to Form 892 to reflect the respective U.S. Publication numbers:

Application 10/728,746 (35) replaced by Patent Application Publication No. 2005/0001261A1;

Application 10/782,975 (37) replaced by Patent Application Publication No. 2004/0232474A1;

Application 10/782,950 (38) replaced by Patent Application Publication No. 2004/0228185A1;

Application 10/783,019 (39) replaced by Patent Application Publication No. 2004/0228181A1;

Application 10/782,974 (40) replaced by Patent Application Publication No. 2004/0229407A1.

***Specification***

6. The disclosure is objected to because of the following informalities: There are minor grammatical informalities in the specification. On page 2, line 18, the specifications reads, "...connection section may connects at least..." It is suggested to change "connects" to "connect."

Appropriate correction is required.

***Drawings***

7. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "50" and "80" have both been used to designate middle line of group labeled "50 (ALC)" on Figure 3 (see Fig. 4). Examiner assumes that applicant intended this line on Fig. 3 to be labeled "80." Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid

abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 102*

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. **Claims 1-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Natori U.S. Patent 6,898,120B2.**

**Regarding independent claim 1**, Natori shows a nonvolatile semiconductor memory device (Fig. 1 [4000]) comprising: a memory array of memory cells arranged in a row direction and a column direction (Fig. 2 [400]).

The memory cell array includes a plurality of element isolation regions (Fig. 5 [STI]; column 4, lines 27-29).

The memory cell includes a first impurity layer (Fig. 4 [SLD]), a second impurity layer (Fig. 4 [BLD]), a channel between the first impurity layer and second impurity layer (Fig. 3 [unlabeled area between N+ and N+]; see column 3, lines 60-63), a word gate (Fig. 4 [412]) and a select gate (Fig. 4 [411]) disposed to face a channel region (column 1, lines 40-41), and a nonvolatile memory element formed between the word gate and channel region (Fig. 4 [410]; column 1, lines 39-40).

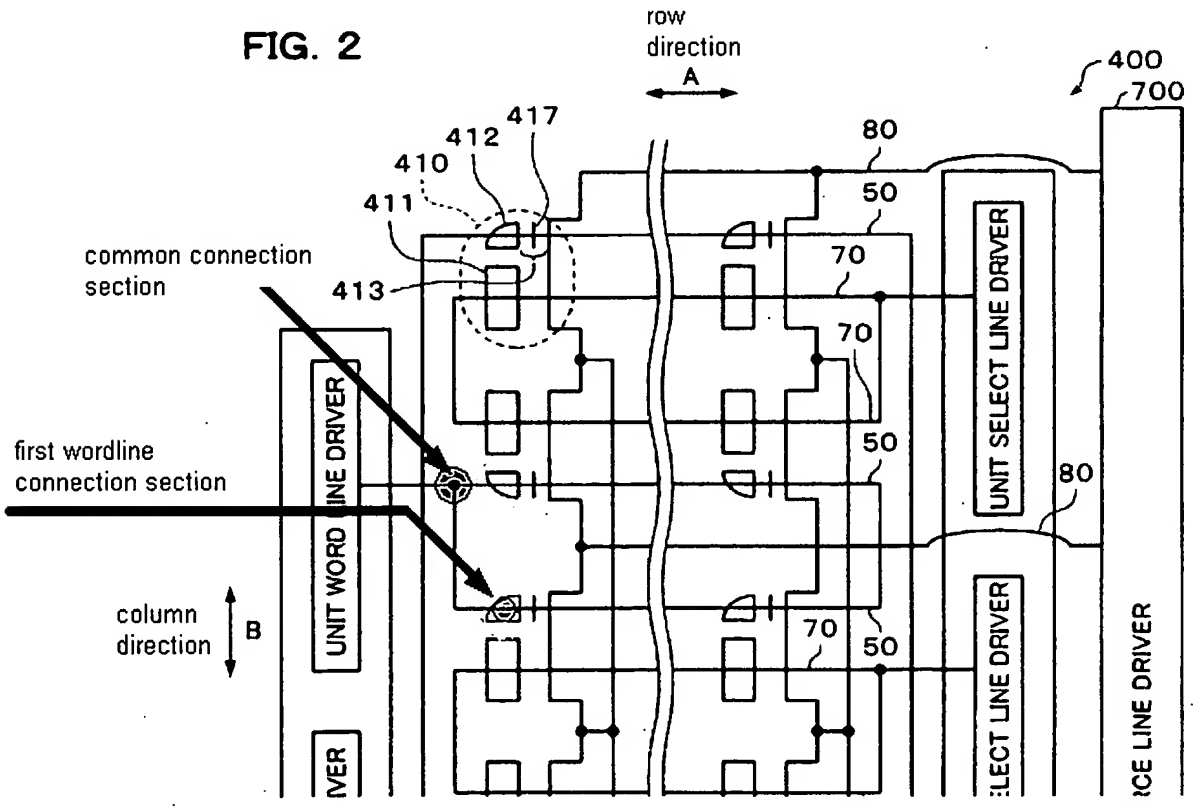
A first wordline connection section connects at least one of a plurality of word gate interconnects, or word lines (Fig. 2 [50]), and at least one of the word gates (Fig. 2 [412]), is disposed above at least on of the element isolation regions (Fig. 5 [412 with respect to STI]).

**Regarding dependent claim 2**, Natori discloses that the memory cell array includes a plurality of memory blocks, wherein the memory blocks includes memory cells, and wherein an operation of erasing data held in each of the memory cells is performed at the same time for each of the memory blocks (column 5, lines 10-11).

**Regarding dependent claim 3**, Natori shows the memory cells (Fig. 2 [410]) include a plurality of word-gate rows (Fig. 2 [50]), each of the word-gate rows is formed by connecting the word gates (Fig. 2 [412]) in the memory cells arranged in the row direction (Fig. 2 [word line 50 hosting a plurality of cells 412 with respect to direction "A"]).

A plurality of common connection sections connect two of the word-gate rows adjacent in the column direction over on of the element isolation regions on which the first wordline connection section is disposed (see Fig. 2 with respect to (Fig. 5 [412 with respect to STI]). See reproduction of Fig. 2 below, as marked up by Examiner to indicate unlabeled points.

FIG. 2



**Regarding dependent claim 4**, Natori shows the first wordline connection section connects at least one of the word gate interconnects (Fig. 2 [50]) with one of the common connection sections (see Fig. 2). See reproduction of Fig. 2 on page 6 of this Office Action, as marked up by Examiner to indicate unlabeled points.

**Regarding dependent claim 5**, Natori shows the memory cells (Fig. 2 [410]) include a plurality of word-gate rows (Fig. 2 [50]), each of the word-gate rows is formed by connecting the word gates (Fig. 2 [412]) in the memory cells arranged in the row direction (Fig. 2 [word line 50 hosting a plurality of cells 412 with respect to direction "A"]).

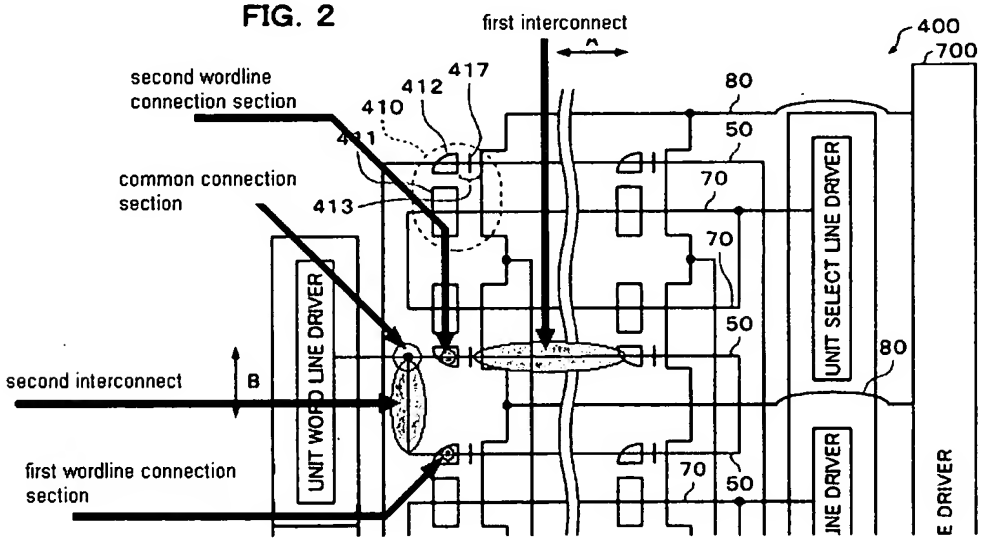
A plurality of common connection sections connect two of the word-gate rows adjacent in the column direction over on of the element isolation regions on which the first wordline connection section is disposed (see Fig. 2 [50] with respect to (Fig. 5 [412 with respect to STI]). See reproduction of Fig. 2 on page 6 of this Office Action, as marked up by Examiner to indicate unlabeled points.

Each of the word gates (Fig. 2 [412]) in the memory block (Fig. 2 [400]) is connected with all of the word gate interconnects (Fig. 2 [50]) in the memory block.

**Regarding dependent claim 6 and 8**, Natori shows the word gate interconnects includes a first interconnect extending along the row direction, and a second interconnect extending along the column direction (see Fig. 2 [50]).

A second wordline connection section which connects one of the common connection sections with the second interconnect is disposed over at least one of the element isolation regions (see Fig. 2[50] with respect to (Fig. 5 [412 with respect to STI]). See reproduction of Fig. 2 below, as marked up by Examiner to indicate unlabeled points.

FIG. 2



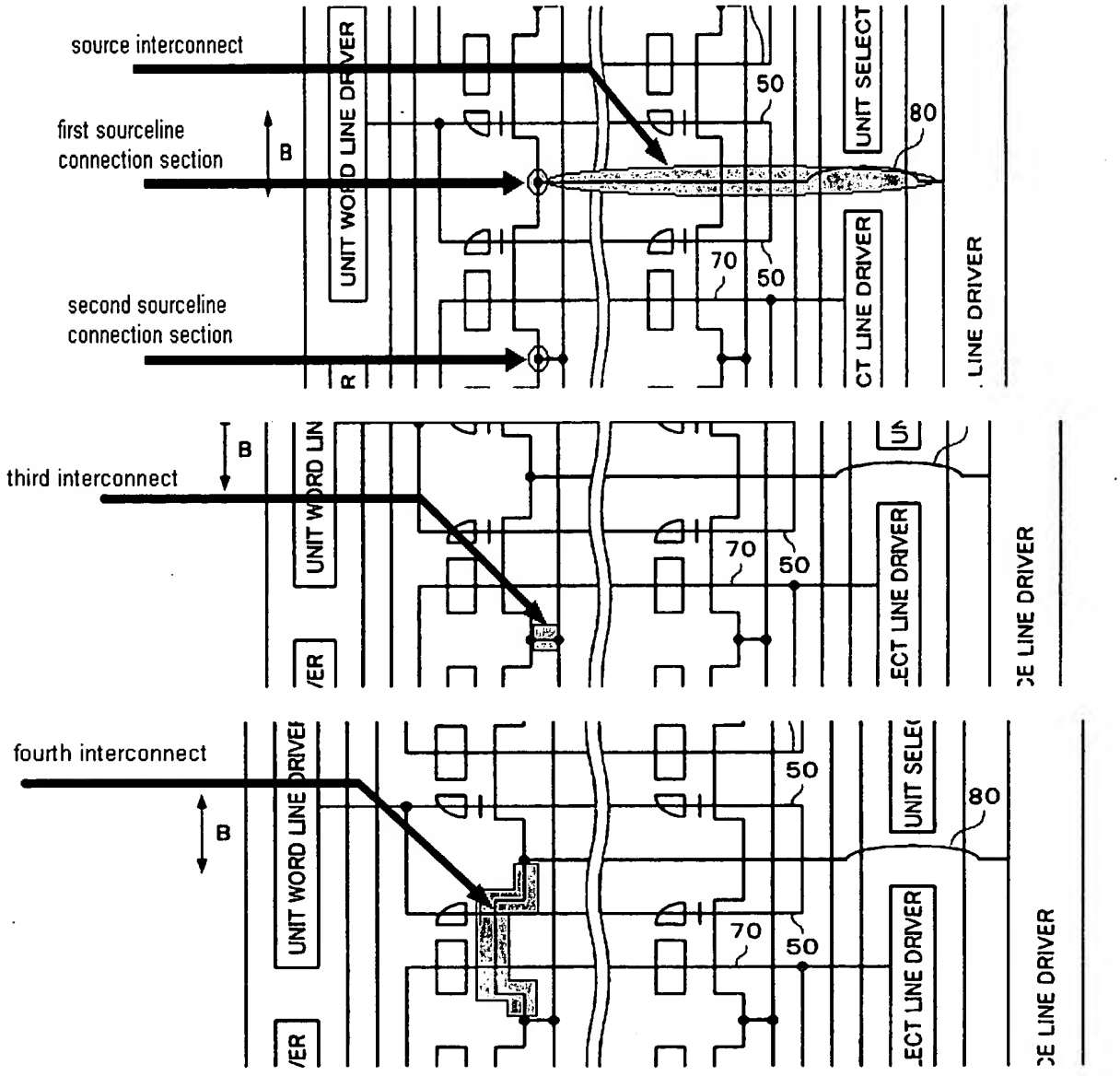

**Regarding dependent claim 7 and 9**, Natori shows a first wordline connection section including a second wordline connection section (see Fig. 2 [50]). See reproduction of Fig. 2 above, as marked up by Examiner to indicate unlabeled points.

**Regarding dependent claim 12**, Natori shows at least one source interconnect (Fig. 2 [80]) and a plurality of first source line connection sections (see Fig. 2 [80]) wherein each of the first source line connection sections connects the source

interconnect with the first impurity layer (see Fig. 2 [connection of 80 and 60] with respect to Fig. 5 [connection of 60 and BLD]).

With respect to **dependent claim 10**, Natori discloses that the diffusion layer BLD and the diffusion layer SLD can be replaced by each other, differing from the structure shown in Fig. 4 (column 4, lines 19-22); therefore, resulting in the recited structure.

**Regarding dependent claim 11 and 13**, Natori shows the source interconnect includes a third interconnect extending along the row direction and a fourth interconnect extending along the column direction (see Fig. 2 [80]) wherein the first source line connection section includes a second source line connection section which connects the third interconnect with the fourth interconnect (see Fig. 2 [80]). See reproduction of Fig. 2 below, as marked up by Examiner to indicate unlabeled points.



***Double Patenting***

10. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Omum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

11. **Claims 1, 3, and 4 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 4 of copending Maemura U.S. Patent Application No. 2004/0232474A1.** Although the conflicting claims are not identical, they are not patentably distinct from each other because both applications similarly claim a non-volatile memory device comprising memory cells with impurity layers, element isolation regions, word gates and select gates, wordline connection sections, word gate interconnects, and common connection sections.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

**Regarding independent claim 1**, Maemura's claim 1 recites a non-volatile semiconductor memory device comprising: a memory cell array in which a plurality of memory cells are arranged in a row direction and a column direction; a plurality of

element isolation regions; wherein each of the memory cells includes one of the source line diffusion layers (**SDL**; a first impurity layer), one of the bitline diffusion layers (**BDL**; a second impurity layer), a channel region between the SDL (first impurity layer) and BDL (second impurity layer), a word gate and a select gate which are disposed to face the channel region, and a nonvolatile memory element formed between the word gate and the channel region; wherein a plurality of word gate wiring layers (wordline connection section) is connected with at least one word gate interconnection (word gate interconnect) which is connected with one of the word gate common connection sections (common connection section) which is connected in common with two word gates above at least one of the element isolation regions.

**Regarding independent claim 3**, Maemura's claim 1 further recites column-wise bit lines, which inherently implies that the word lines are arranged in rows. Thus, the word-gates, which are connected to the word lines, are arranged in the row direction forming word-gate rows. Maemura's claim 1 further recites that each of the word gate common connection sections (common connection sections) is connected in common with the two word gates over at least one element isolation region; wherein "the two word gates" is recited to be two word gates adjacent in the column direction. Maemura's claim 4 recites that the word gate common connection sections (common connection sections) are formed along the column direction.

**Regarding independent claim 4**, Maemura's claim 1 further recites a plurality of word gate wiring layers (wordline connection section) is connected with at least one

word gate interconnection (word gate interconnect) which is connected with one of the word gate common connection sections (common connection section).

12. **Claims 1, 3, and 4 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 2, and 5 of copending Owa U.S. Patent Application No. 2004/0229407A1.** Although the conflicting claims are not identical, they are not patentably distinct from each other because both applications similarly claim a non-volatile memory device comprising memory cells with impurity layers, element isolation regions, word gates and select gates, wordline connection sections, word gate interconnects, and common connection sections..

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

**Regarding independent claim 1**, Owa's claim 1 recites a non-volatile semiconductor memory device comprising: a memory cell array in which a plurality of memory cells are arranged in a row direction and a column direction; a plurality of element isolation regions; wherein each of the memory cells includes one of the source line diffusion layers (**SDL**; a first impurity layer), one of the bitline diffusion layers (**BDL**; a second impurity layer), a channel region between the SDL (first impurity layer) and BDL (second impurity layer), a word gate and a select gate which are disposed to face the channel region, and a nonvolatile memory element formed between the word gate and the channel region; wherein a plurality of word gate wiring layers (wordline

connection section) is connected with at least one word gate interconnection (word gate interconnect) which is connected with one of the word gate common connection sections (common connection section) which is connected in common with two adjacent word gates above at least one of the element isolation regions.

**Regarding independent claim 3**, Owa's claim 1 further recites memory cells with word gates in the memory array arranged in a column direction and a row direction. Word lines are well-known in the art to be oriented in a row direction and to be connected to word gates. Thus, the word-gates, which are connected to the word lines, are arranged in the row direction forming word-gate rows. Owa's claim 1 further recites that each of the word gate common connection sections (common connection sections) is connected in common with the two adjacent word gates over at least one element isolation region. Owa's claim 5 recites that the word gate common connection sections (common connection sections) are arranged along the column direction.

**Regarding independent claim 4**, Owa's claim 1 further recites a plurality of word gate wiring layers (wordline connection section) is connected with at least one word gate interconnection (word gate interconnect) which is connected with one of the word gate common connection sections (common connection section).

***Conclusion***

When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs.

A shortened statutory period for response to this action is set to expire three months and zero days from the date of this letter. Failure to respond within the period for response will cause this application to become abandoned (see MPEP 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGS

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